Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.111”**

**.111”**

**Top Material: Al**

**Backside Material: Au/Cr/Ni/Au**

**B = .020” X .030”**

**E = .020” X .026”**

**Backside Potential: Collector**

**Process: CP117**

**APPROVED BY: DK DIE SIZE .111” X .111” DATE: 9/8/21**

**MFG: CENTRAL SEMI THICKNESS .011” P/N: 2N6039**

**DG 10.1.2**

#### Rev B, 7/19/02